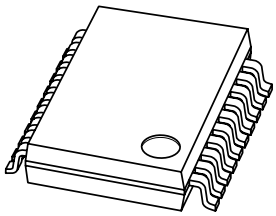
查询PESD5V2S18U供应商

DATA SHEET



PESD5V2S18U
ESD protection array

Product specification

2003 Apr 28

Philips
Semiconductors

PHILIPS

ESD protection array PESD5V2S18U

FEATURES

- Uni-directional ESD protection of up to 18 lines
- Maximum peak reverse power: P_{PP} = 100 W at t_p = 8/20 μs
- Low clamping voltage: V_{CL} = 12 V max. at I_{ZSM} = 10 A
- Low leakage current: I_R = 100 nA typ. at V_{RWM} = 5.2 V
- IEC 61000-4-2, level 4 (ESD); 15 kV (air) and 8 kV (contact).

APPLICATIONS

- Printer parallel ports
- Computers and peripherals
- Communication systems.

DESCRIPTION

Monolithic ESD protection device designed to protect up to 18 transmission or data lines from the damage caused by electrostatic discharge (ESD) and surge pulses.

PINNING

PIN	DESCRIPTION
1 to 5	cathode (k1 to k5)
6 and 16	common anode (a1; a2)
7 to 15	cathode (k6 to k14)
17 to 20	cathode (k15 to k18)

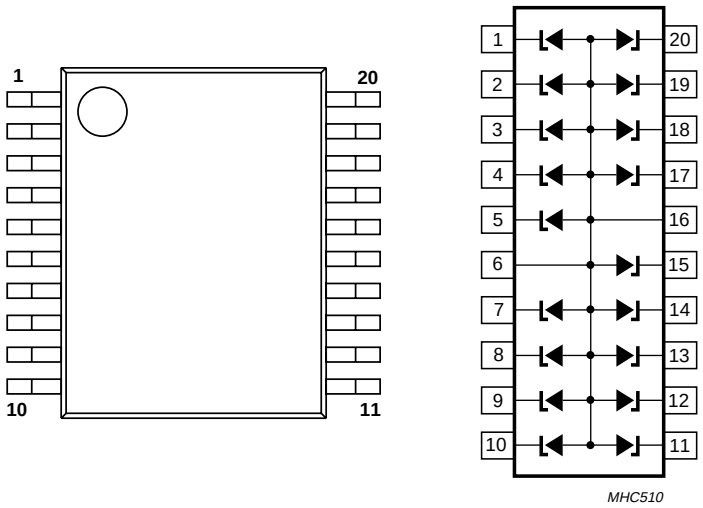


Fig.1 Simplified outline (SSOP20; SOT339-1) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{PP}	non-repetitive peak reverse current	t_p = 8/20 μs	–	10	A
P_{PP}	non-repetitive peak reverse power dissipation	t_p = 8/20 μs	–	100	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–65	+150	°C
	electrostatic discharge voltage	IEC 61000-4-2 (contact discharge)	30	–	kV
		HBM MIL-Std 883	10	–	kV

ESD standards compliance

IEC 61000-4-2, level 4 (ESD)	>15 kV (air); >8 kV (contact)
HBM MIL-Std 883, class 3	>4 kV

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	one or more diodes loaded	135	K/W

Note

1. Refer to SOT339-1 standard mounting conditions.

ELECTRICAL CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{RWM}	crest working reverse voltage		–	–	5.2	V
I_R	reverse current	V_{RWM} = 5.2 V	–	0.1	1	µA
V_{CL}	clamping voltage	I_{ZSM} = 3 A; t_p = 8/20 µs; see Fig.5	–	–	8	V
		I_{ZSM} = 10 A; t_p = 8/20 µs; see Fig.5	–	–	12	V
V_{BR}	breakdown voltage	I_Z = 5 mA	6.4	6.8	7.2	V
r_{diff}	differential resistance	I_Z = 1 mA	–	–	40	Ω
		I_Z = 5 mA	–	–	8	Ω
C_d	diode capacitance	V_R = 0; f = 1 MHz; see Fig.4	–	100	–	pF

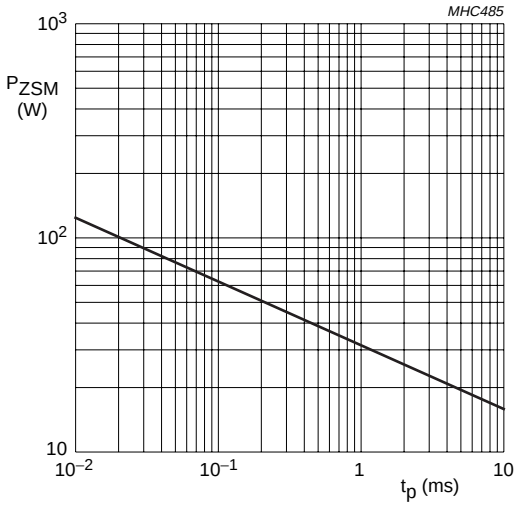


Fig.2 Maximum non-repetitive peak reverse power as a function of pulse duration.

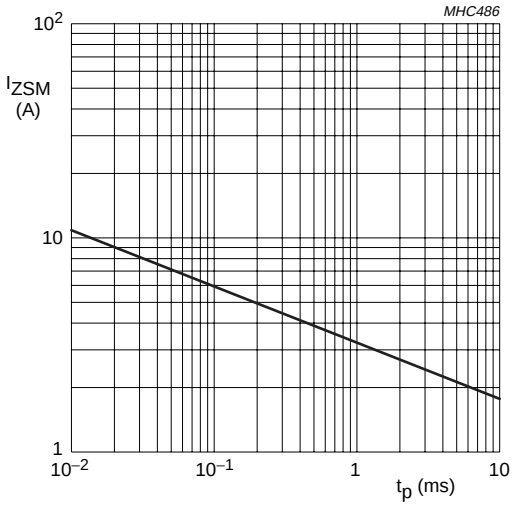
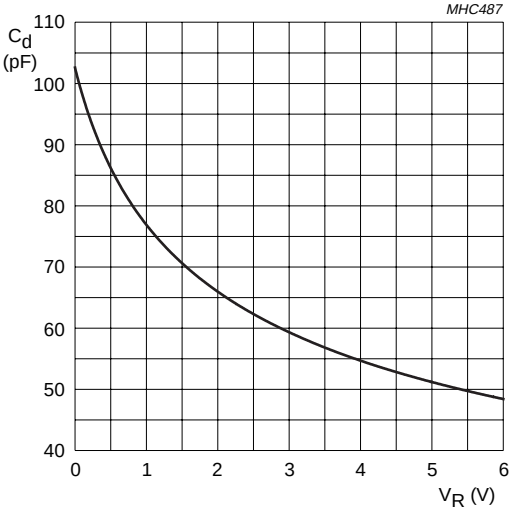
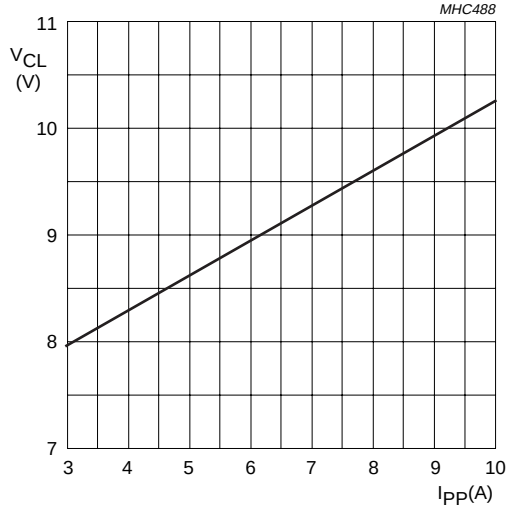


Fig.3 Maximum non-repetitive peak reverse current as a function of pulse duration.



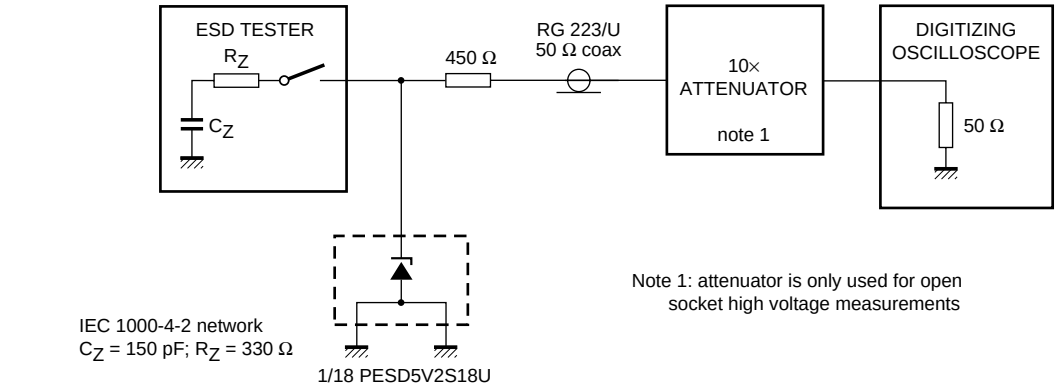
f = 1 MHz; T_{amb} = 25 °C

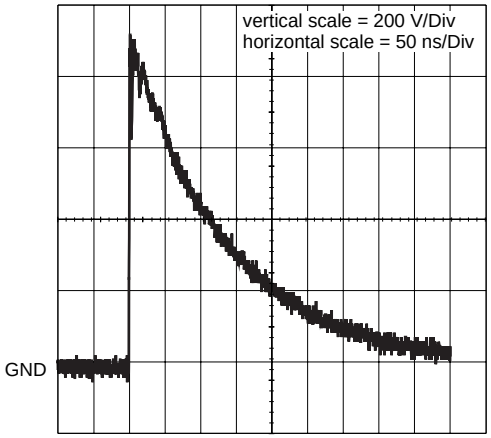
Fig.4 Diode capacitance as a function of reverse voltage; typical values.



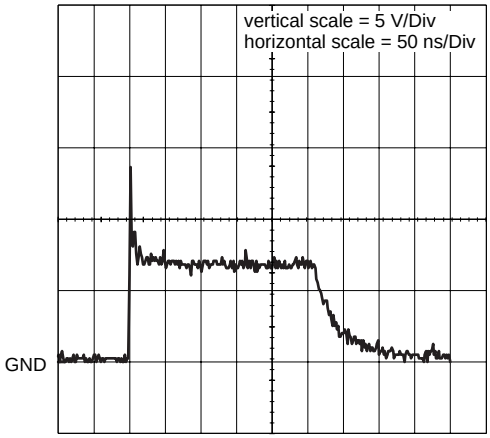
t_p = 8/20 μs

Fig.5 Clamping voltage as a function of peak reverse pulse current; typical values.

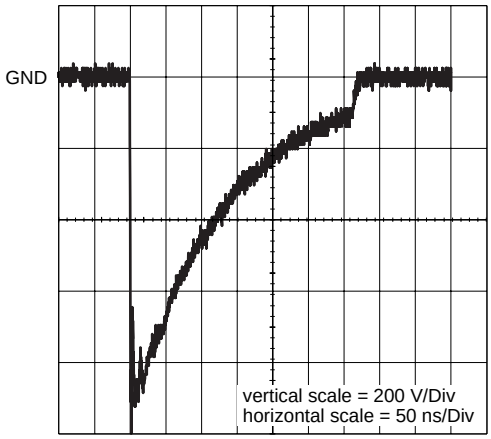




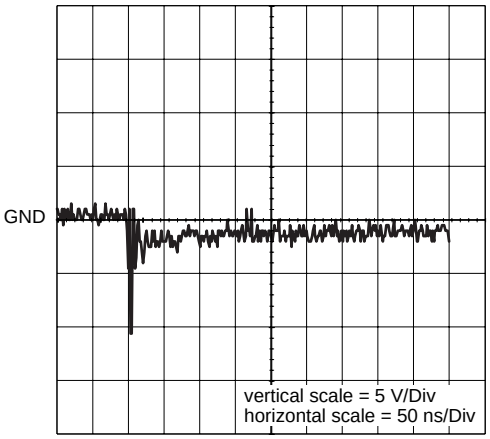
unclamped +1 kV ESD voltage waveform
(IEC 1000–4–2 network)



clamped +1 kV ESD voltage waveform
(IEC 1000–4–2 network)



unclamped –1 kV ESD voltage waveform
(IEC 1000–4–2 network)



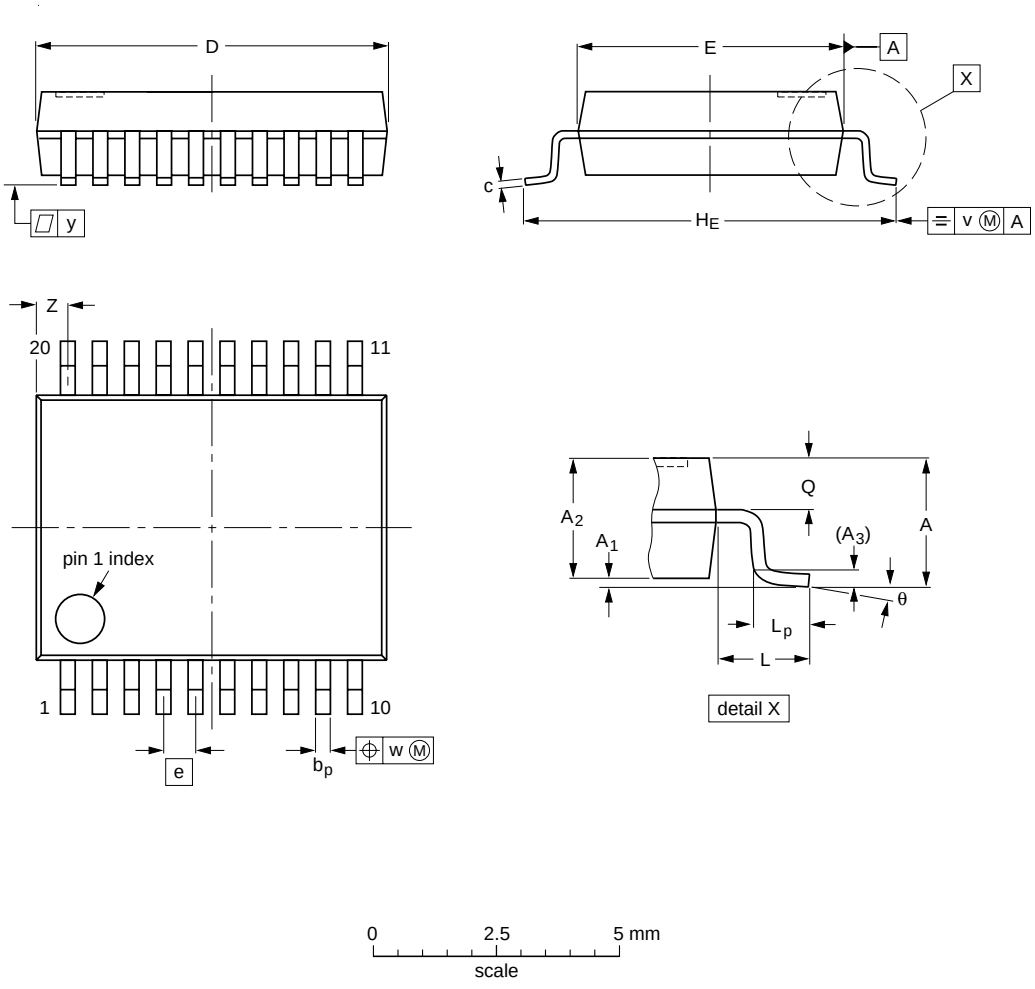
clamped –1 kV ESD voltage waveform
(IEC 1000–4–2 network)

MHC489

Fig.6 ESD clamping test set-up and waveforms.

PACKAGE OUTLINE

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm **SOT339-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8^o 0^o

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT339-1		MO-150				~~99-12-27~~ 03-02-19

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